Claims

What is claimed is:

1. A method for operating a buffer memory, the buffer having a plurality of entries, the entries being subject of at least one process to work on, said method comprising:

generating for each of said entries validation information which is evaluable for the status of an entry relative to its further processing by said at least one process.

2. The method according to claim 1 in which said validation information is specific for each of a plurality of processes and indicating if a respective entry can be subjected to a respective process, or not.

3. The method according to claim 1, comprising generating said validation information by combinatorial logic processing a process-related IN-pointer and OUT-pointer.

4. The method according to claim 3 in which said buffer memory is a window buffer able to be filled with processing instructions, said processes being at least two of dispatching new instructions to said window buffer, retiring instructions from said window buffer by a commit process, or purging at least one instruction from said window buffer.

5. The method according to claim 3 for use in managing queues.

6. A buffer storage device having a plurality of n entries, the entries being subject of at least one process to work on, and comprising:

means for generating for each of said entries validation information which is evaluable for the status of an entry relative to its further processing by said at least one process.

7. The buffer storage device of claim 6 in which said validation information is specific for each of a plurality of processes and indicating if a respective entry can be subjected to a respective process, or not.

8. The buffer storage device of claim 7 in which the means for generating said validation information is a combinatorial logic processing process-related values of pointers.

9. A sub-unit for use in microprocessor devices having at least one storage device according to claim 6.

10. A microprocessor device having at least one sub-unit according to claim 9.

11. A computer system having a microprocessor device according to claim 10.

12. A computer system having a microprocessor device, said microprocessor device having at least one sub-unit, said at least one sub-unit having one or more storage devices, at least one storage device of said one or more storage devices having a plurality of n entries, the entries being subject of at least one process to work on, and said at least one storage device comprising:

means for generating for each of said entries validation information which is evaluable for the status of an entry relative to its further processing by said at least one process.

13. The computer system of claim 12, in which said validation information is specific for each of a plurality of processes and indicating if a respective entry can be subjected to a respective process, or not.

14. The computer system of claim 13, in which the means for generating said validation information is a combinatorial logic processing process-related values of pointers.

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